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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,313	04/13/2004	Zhenjiang Cui	007034 USAP03/DSM/BCVD/J	5975

7590 11/23/2004

APPLIED MATERIALS, INC.
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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 11/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,313	CUI ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on April 13th, 2004 is acceptable.

Drawings

2. The formal drawings filed on August 23rd, 2004 are acceptable.

Information Disclosure Statement

3. The Information Disclosure Statement filed on April 13th, 2004 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Ross (U.S. Patent 6,548,899).

In re claim 1, **Ross** discloses a method for treating silicon nitride (Si_xN_y) films that comprises: electron beam treating the silicon nitride film (col. 2, lines 55-65 and col. 5, lines 54-60).

On the surface of the substrate is an optional pattern of raised lines, such as metal, oxide, nitride or oxynitride lines which are formed by well known lithographic techniques. Suitable materials for the lines include silica, silicon nitride, titanium nitride, tantalum nitride, aluminum, aluminum alloys, copper, copper alloys, tantalum, tungsten and silicon oxynitride. These lines form the conductors or insulators of an integrated circuit. Such are typically closely separated from one another at distances of about 20 micrometers or less, preferably 1 micrometer or less, and more preferably from about 0.05 to about 1 micrometer.

The film may also be cured by exposing the surface of the substrate to a flux of electrons. Whether the film is cured by electron beam exposure or is cured by other means such as heating or exposure to UV light, the surface of the dielectric film is exposed to sufficient electron beam exposure to remove substantially all moisture and contaminants from the surface of the dielectric layer.

In re claim 2, **Ross** discloses that the method of claim 1, which further comprises heating the film to a temperature in a range from about 25° C to about 1050° C (col. 5, line 61 to col. 6, line 11).

Preferably the electron beam exposure is done at a vacuum in the range of from about 10^{-5} to about 10^{2} torr, and with a substrate temperature in the range of from about 25° C. to about 1050° C. When the electron beam is used both for

In re claim 3, **Ross** discloses that the step of electron beam treating includes exposing the film to electron beam current at doses in a range from about 100 $\mu C/cm^2$ to about 5,000 $\mu C/cm^2$ (col. 6, lines 12-21).

When the electron beam is used both for dielectric curing and surface treatment, the electron beam dose will fall into the range of from about 1 to about 100,000 $\mu C/cm^2$, preferably from about 100 to about 10,000$\mu C/cm^2$, and more preferably from about 1 to about 8,000 $\mu C/cm^2$. The dose and energy selected will be proportional to the thickness of the films to be processed. When the electron beam is used as a dielectric surface treatment, energy and doses will fall into the ranges of about 0.5 to about 3 KeV and about 100 to about 5,000 $\mu C/cm^2$, respectively. The appropriate doses and

In re claim 4, **Ross** discloses that the step of electron beam treating further includes exposing the film from about 0.5 minute to about 120 minutes (col. 6, lines 12-42).

about 1000 Å from the surface. Generally the exposure will range from about 0.5 minute to about 120 minutes, and preferably from about 1 minute to about 60 minutes. The

In re claim 5, **Ross** discloses that the step of electron beam treating comprises placing the film in an ambient gas in a chamber wherein the electron beam is formed between a cathode and an anode, and providing a cathode voltage in range form about -.5 KV to about –10 KV (col. 6, lines 12-42).

In re claim 6, **Ross** discloses wherein the ambient gas is one or more of N2, H2, Ar, O2, or any combination of these gases (col. 6, lines 40-42).

inches. The gaseous ambient in the electron beam system chamber may be nitrogen, hydrogen, argon, oxygen, or any combinations of these gases.

In re claim 7, **Ross** discloses that a pressure of the ambient gas in the chamber and a working distance between the cathode and the anode are maintained so that arcing does not occur between the cathode and the anode (col. 7, line 28 to col. 8, line 7).

In re claim 8, **Ross** discloses wherein the pressure of the ambient gas in the chamber is maintained at one or more levels that provide a substantially constant electron beam current during at least one treatment period (col. 7, lines 28 to col. 8, line 7).

5. Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by S. Inaba et al. (Increase of Parasitic Resistance in Shallow P+ Extension with SiN Sidewall Process and

Its Improvement by Ge Preamorphization for Sub-0.25-μm pMOSFET's" IEEE Trans. Electr.Dev., Vol. 46, No. 6, June 1999, pp. 1218-1224).

In re claim 9, **Ross** discloses a method for fabricating a pMOSFET that comprises steps of (pages 1218-1219 and FIG. 1): oxidizing a gate; forming a gate electrode; implanting to form shallow source/drain extensions;

> RECENT progress in the miniaturization of Si-MOSFET's has reached the 0.1-μm region in gate length [1]–[3]. With such a small gate length, both suppression of the short-channel effect (SCE) and reduction of the parasitic effects are strongly required to achieve high performance [4]. One of the key issues for realizing high performance sub-0.25-μm CMOS is to form a shallow source/drain (S/D) extension region with low parasitic resistance (R_{par}). This is a severe restriction, especially for pMOSFET's, because it is more difficult to

forming a SiN gate sidewall; implanting to form source/drain deep junctions; and activating the source/drain.

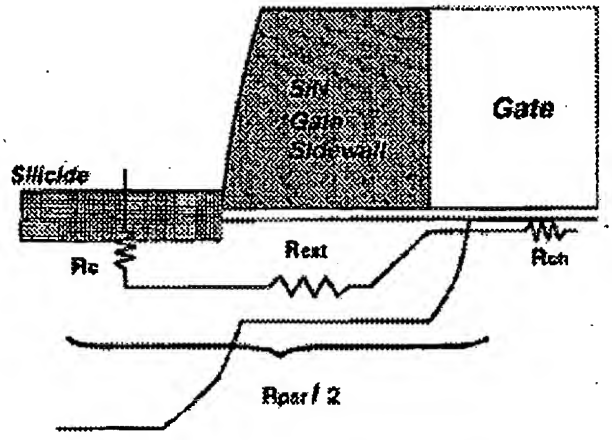

Fig. 1. Schematic cross section of source/drain extension structure of MOSFET. R_{ext} contains sheet resistance R_{sh}, spreading resistance R_{sp}, and accumulation resistance R_{ac}.

realize a shallow junction depth and low resistance in p^+ extension region than in n^+ extension.

Typical schematic cross section of the extension structure of MOSFET with SALICIDE process is shown in Fig. 1. The source/drain electrode is divided into two parts by SiN gate sidewall; i.e., the extension region and the deep junction region. In this case, R_{par} is also composed of two parts. One is

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
November 18th, 2004

W. David Coleman
Primary Examiner